

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Priority Application Serial No. .... 10/280,757  
Priority Filing Date ..... October 24, 2002  
Inventor ..... Luan C. Tran  
Assignee ..... Micron Technology, Inc.  
Priority Group Art Unit ..... 2822  
Priority Examiner ..... Vu Anh Le  
Attorney's Docket No. .... MI22-2429  
Title: A 6F<sup>2</sup> DRAM Array, A DRAM Array Formed On A Semiconductive Substrate, A  
Method Of Forming Memory Cells In A 6F<sup>2</sup> DRAM Array And A Method Of  
Isolating A Single Row Of Memory Cells In A 6F<sup>2</sup> DRAM Array

**INFORMATION DISCLOSURE STATEMENT**

References -- See attached Form PTO-1449


In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a divisional application of co-pending application Serial No. 10/280,757, filed October 24, 2002, upon which the above-identified application relies for a priority date under 35 U.S.C. § 120. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. § 1.98(d) and MPEP § 609(2). As a courtesy, Applicant submits copies of the cited foreign reference and articles (only) for review.

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: Nov. 13, 2003

By:   
Deepak Malhotra  
Reg. No. 33,560

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-2429	SERIAL NO. Filed Herewith		
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Luan C. Tran			
				FILING DATE Filed Herewith	GROUP Unassigned		
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,175,146 B1	01/16/01	Lane et al.			
	AB	6,165,833	12/26/00	Parekh et al.			
	AC	6,153,899	11/28/00	Ping			
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	AF	5,994,749	11/30/99	Oda			
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	AI	5,880,989	03/09/99	Wilson et al.			
	AJ	5,828,615	10/27/98	Mukunoki et al.			
	AK	5,716,864	02/10/98	Abe			
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
							Yes    No
	AL	WO96/39713	12/12/96	PCT			
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	AO						
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AR		C.T. Liu et al., <i>Multiple Gate Oxide Thickness for 2GHz System-on-A-Chip Technologies</i> , 1998 IEEE, pages 21.2.1-21.2.4 (4 pages).				
	AS		Lian-Hoon Ko et al., <i>The Effect of Nitrogen Incorporation into the Gate Oxide by Using Shallow Implantation of Nitrogen and Drive-in Process</i> , 1998 IEEE, pages 32-35 (4 pages).				
	AT		Brian Doyle et al., <i>Simultaneous Growth of Different Thickness Gate Oxides in Silicon CMOS Processing</i> , 1995 IEEE, pages 301-302 (2 pages).				
EXAMINER				DATE CONSIDERED			
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				FILING DATE Filed Herewith		GROUP Unassigned	
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
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	AB	5,680,344	10/21/97	Seyyedy			
	AC	5,677,865	10/14/97	Seyyedy			
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	AJ	5,880,991	3/1999	Hsu et al.			
	AK						
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
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	AL						
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	AO						
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AR		T. Kuroi et al., <i>The Effects of Nitrogen Implantation Into P+ Poly-Silicon Gate On Gate Oxide Properties</i> , 1994 IEEE, pages 107-108				
			(2 pages).				
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	AT						
EXAMINER				DATE CONSIDERED			
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